REMARKS/ARGUMENTS

Claims 1, 3, 4, 6, 8, 9 and 11-23 are pending herein. Claims 1, 6, 12 and 17 have been amended as supported by page 12, lines 8-27 of the specification, for example. New claims 22 and 23 have been added corresponding directly to previously cancelled claims 2 and 7. Applicants respectfully submit that no new matter has been added.

1. Claims 1, 3-6 and 8-11 were rejected under §103(a) over Yasunori in view of Duggal. To the extent that this rejection may be applied against the amended claims, it is respectfully traversed.

Claims 1 and 6 recite, in relevant part, an EL element comprising an EL part. The EL part comprises a first electrode, an insulating layer pattern, an EL layer, and a second electrode. The insulating layer pattern is positioned between the first electrode layer and the EL layer or between the EL layer and the second electrode.

The Examiner is respectfully requested to note that fluorescent emission takes place at positions corresponding to the openings in the insulating layer pattern 11, while fluorescent emission does not take place at the positions other than the openings (specification, page 12, lines 8-10). Accordingly, in this case, luminescence can be provided in the opening pattern (specification, page 12, lines 10-11). On the other hand, during energization, a fluorescent emission pattern corresponding to the insulating layer pattern 11 in the EL element 12 is visible, and, in the parts other than the fluorescent emission pattern, the print can be viewed (specification, page 12, lines 20-24). According to this method, the fluorescent emission may be constructed so as to take place even on the whole area, or the fluorescent emission may be constructed for color display applications (specification, page 12, lines 24-27).

Yasunori discloses, in Fig. 2, the use of an insulator film 8 surrounding the lower electrode 3. Yasunori discloses, in paragraph [0041], that in such a light emitting device, it is assumed that the insulator film 8 is formed in the circumference of the lower electrode 3, and that these components are further provided in the sealing layer 9 in the state of a wrap. Accordingly, the insulator film 8 of Yasunori is an ordinary insulator and is formed in the circumference of the lower electrode 3 under the electron hole transporting layer 4. Further, the Examiner is respectfully requested to note that because the insulator layer 8 of Yasunori does not include any form of pattern, as in the present invention, there would have been no reason for one skilled in the art to place the insulator layer 8 of Yasunori between the first electrode and the EL layer or between the EL layer and the second electrode. Therefore, Yasunori fails to disclose or suggest that the insulator layer 8 can or should be located between the first electrode and the EL layer or between the EL layer and the second electrode, and that the insulator layer 8 can or should be an insulating layer pattern.

Applicants respectfully submit that in light of the foregoing, the insulator layer 8 of Yasunori cannot be interpreted in such a manner that it could be considered comparable to the insulating layer pattern recited in claims 1 and 6. Applicants respectfully submit that this point is made even clearer by the Examiner's differing interpretation of the insulator layer 8 of Yasunori throughout the present Office Action. For example, the Examiner refers to the insulator layer 8 as "a light transparent layer (8)" in the last three lines on page 5 of the Office Action where the Examiner further explains that "Yasunori does not disclose the light transparent layer is a pattern layer." Further, the Examiner indicates in the first line on page 7 and in line 14 on page 8 of the Office Action that the insulator layer 8 of Yasunori is a "design layer." In any event, the Examiner's assertion, in the last line on page 5 of the

Office Action, that Yasunori does not disclose that the light transparent [i.e., insulator] layer 8 is a pattern layer is technically correct.

Duggal, used by the Examiner only for alleged disclosure of a barrier layer having a water vapor barrier property, fails to disclose or suggest any form of insulating layer pattern located between a first electrode and an EL layer or between an EL layer and a second electrode, as claimed. Therefore, Duggal fails to overcome the deficiencies of Yasunori.

For at least the foregoing reasons, Applicants respectfully submit that the EL element recited in claims 1 and 6 would not have been obvious to one skilled in the art provided with the disclosures of Yasunori and Duggal. Since claims 3-4, 11 and 22 depend directly from claim 1 and claims 8, 9 and 23 depend directly from claim 6, those claims are also believed to be allowable over the applied prior art. Accordingly, reconsideration and withdrawal of the present rejection are respectfully requested.

2. Claims 12-15 and 17-20 were rejected under §103(a) over Yasunori in view of Bellmann. To the extent that this rejection may be applied against the amended claims, it is respectfully traversed.

Claims 12 and 17 recite, in relevant part, a display using an EL element, said EL element comprising a first electrode, an insulating layer pattern, an EL layer, and a second electrode. The insulating layer pattern is between the first electrode and the EL layer or between the EL layer and the second electrode.

As discussed in further detail above, Yasunori fails to disclose or suggest that the insulator layer 8 can or should be located between the first electrode and the EL layer or between the EL layer and the second electrode, and that the insulator layer 8 can or should be an insulating layer pattern. The Examiner appears to acknowledge at least the latter fact in his statement in the last three lines on page 5 of the Office Action that Yasunori discloses "a light transparent layer (8)" (i.e., the insulator layer

(8)) and that "Yasunori does not disclose that the light transparent layer is a pattern layer." Accordingly, even though Applicants respectfully disagree with the Examiner's interpretation that the insulator layer 8 of Yasunori is a light transparent layer, it is agreed that Yasunori does not disclose that the layer is a pattern layer.

Bellmann, used by the Examiner only for its alleged disclosure of a light transparent pattern layer, fails to disclose or suggest any form of an insulating layer pattern that is between a first electrode and an EL layer or between an EL layer and the second electrode, as claimed. Accordingly, Bellmann fails to overcome the deficiencies of Yasunori.

For at least the foregoing reasons, a display using an EL element as recited in claims 12 and 17 would not have been obvious to one skilled in the art provided with the disclosures of Yasunori and Bellmann. Since claims 13-15 depend either directly or indirectly from claim 12 and claims 18-20 depend either directly or indirectly from claim 17, those claims are also believed to be allowable over the applied prior art. Accordingly, reconsideration and withdrawal of the present rejection are respectfully requested.

3. Claims 16 and 21 were rejected under §103(a) over Yasunori and Bellmann in view of Duggal. Applicants respectfully submit that the arguments submitted above distinguish claims 12 and 17 from Yasunori and Bellmann. Since Duggal fails to overcome the deficiencies of Yasunori and Bellmann, and since claim 16 depends directly from claim 12 and claim 21 depends directly from claim 17, those claims are also believed to be allowable over the applied prior art. Accordingly, reconsideration and withdrawal of the present rejection are respectfully requested.

If the Examiner believes that contact with Applicants' attorney would be advantageous toward the disposition of this case, the Examiner is herein requested to call Applicants' attorney at the phone number noted below.

The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-1446.

Respectfully submitted,

March 10, 2008
Date

Stephen P. Burr
Reg. No. 32,970

Timothy D. Evans
Reg. No. 50,797

SPB/TE/tlp

BURR & BROWN
P.O. Box 7068
Syracuse, NY 13261-7068

Customer No.: 025191
Telephone: (315) 233-8300
Facsimile: (315) 233-8320